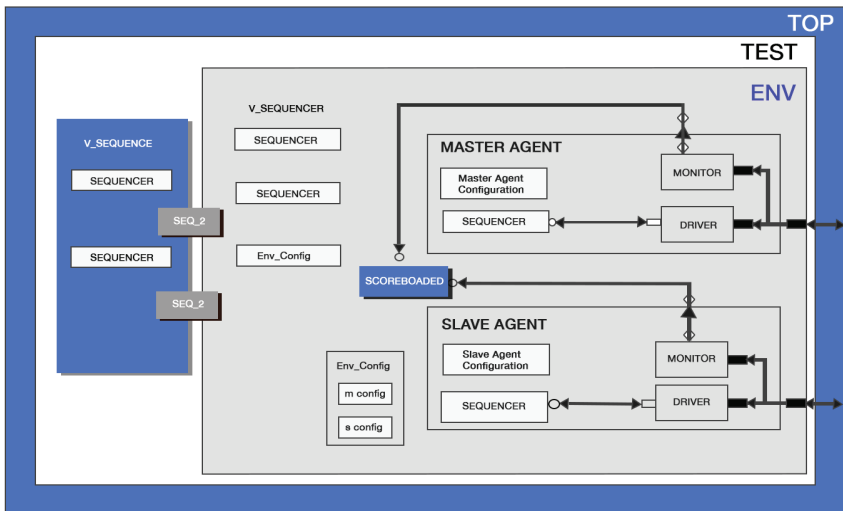


Overview

Chiplogic Semiconductor offers the AMBA High-performance Bus (AHB) which support both Master and Slave configuration UVM VIP. It supports AMBA 2.0. It is highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment.



Features

- » **Ease of use:** VIP is architected to allow user to generate large set of directed/constrain-randomized stimulus with very less effort.
- » **Pipelined Support:** Components are architected to support pipelined nature of AHB spec. support only aligned transfers.
- » **Transaction Log:** An exhaustive transaction log shows time-stamped transaction from each channel, this allows easy analysis and debug
- » **Coverage:** All possible cover points and cover bins are implemented to get coverage measure without extra effort
- » **Checkers:** System Verilog based assertions are coded to check every protocol feature and report errors to catch issues and debug with ease

Features

- » Compliant to AMBA specifications 2.0
- » User can set VIP as master or slave and agent as active or passive without changing testbench, and determine, during run time, which instance to instantiate.
- » Supports aligned transfers
- » Supports all legal data and address widths
- » Configurable option to use automatic slave responses
- » Can introduce delay during transfer
- » Can support any number of agents
- » Can support OKAY, ERROR, SPLIT and RETRY responses
- » Exhaustive sequenc library
- » Coverage
- » Protocol checkers

Language and Methodology

- » System Verilog & UVM

Deliverables

- » Encrypted VIP Source code
- » Plaintext Sequence Library
- » Example test bench and test cases
- » User guide

For more information on our Semiconductor IP's reach out to us at:
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