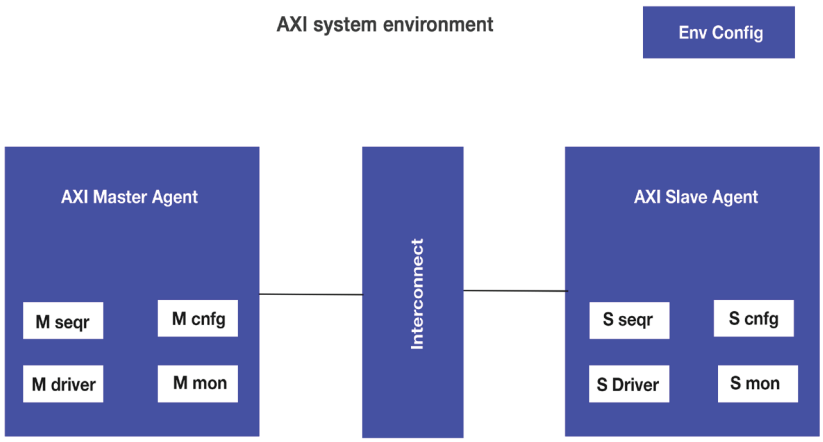
AXI 4.0 VIP

CHIPLOGIC

Overview

Chiplogic Semiconductor offers the AMBA Advanced extensible Interface (AXI) 4.0/3.0 which support both Master and Slave configuration UVM VIP. This is highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment.



Features

- » **Ease of use:** VIP is architected to allow user to generate large set of directed/constrain-randomized stimulus with very less effort.
- » **Pipelined Support:** Components are architected to support pipelined nature of AXI spec. support only aligned transfers.
- » **Transaction Log:** An exhaustive transaction log shows time-stamped transaction from each channel, this allows easy analysis and debug
- » **Coverage:** All possible cover points and cover bins are implemented to get coverage measure without extra effort
- » **Checkers:** System Verilog based assertions are coded to check every protocol feature and report errors to catch issues and debug with ease

Features

- » Compliant to AXI 4.0
- » Supports unaligned transfers, Write Strobe, Narrow Transfers
- » Supports Configurable Multiple outstanding transfers
- » In order and out-of-order transfers
- » Parrallel write and read operations
- » Data before address
- » Atoic Access, QOS
- » Exhaustive sequence library
- » Coverage
- » Protocol checkers

Language and Methodology

- » System Verilog & UVM

Deliverables

- » Encrypted VIP Source code
- » Plaintext Sequence Library
- » Example test bench and test
- » cases
- » User guide

For more information on our Semiconductor IP's reach out to us at:
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