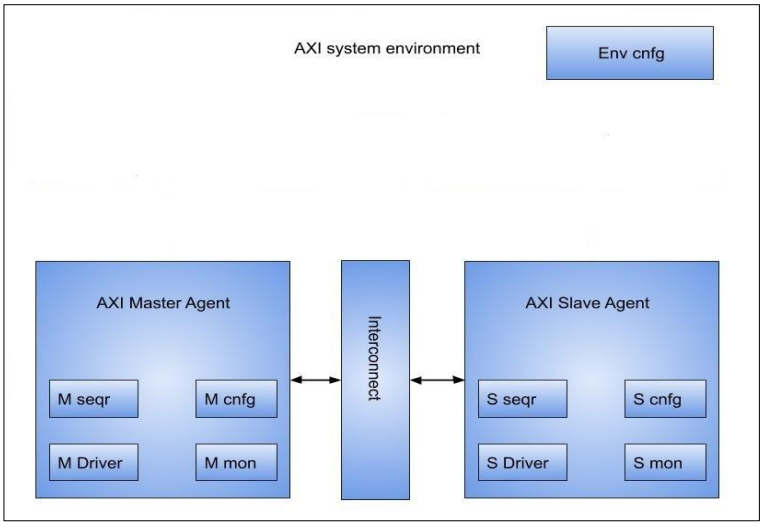
AXI 4.0 VIP

Overview

Chiplogic Semiconductor offers the AMBA Advanced extensible Interface (AXI) 4.0/3.0 which support both Master and Slave configuration UVM VIP. This is highly flexible and configurable verification IP, which can be easily integrated into any SOC verification environment.

Block Diagram



Feature Description

Ease of use: VIP is architected to allow user to generate large set of directed/constrain-randomized stimulus with very less effort.

Pipelined Support: Components are architected to support pipelined nature of AXI spec. Supports out-of-order

Transaction Log: An exhaustive transaction log shows time-stamped transaction from each channel, this allows easy analysis and debug

Coverage: All possible cover points and cover bins are implemented to get coverage measure without extra effort

Checkers: System Verilog based assertions are coded to check every protocol feature and report errors to catch issues and debug with ease

Features

- Compliant to AXI 4.0
- Supports unaligned transfers, Write Strobe, Narrow Transfers
- Supports Configurable Multiple Outstanding Transfers
- In order and Out-of-order Transfers
- Parallel Write and Read operations
- Data before address
- Atomic Access, QOS,
- Exhaustive sequence library
- Coverage
- Protocol checkers

Language and Methodology

- System Verilog & UVM

Deliverables

- Encrypted VIP Source code
- Plaintext Sequence Library
- Example test bench and test cases
- User guide

Contacts

sales@chiplogictech.com
www.chiplogictech.com