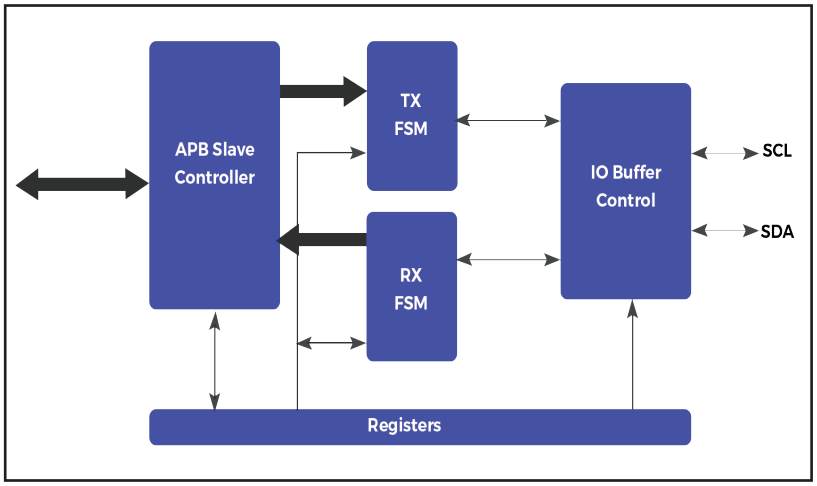
I2C Semiconductor IP

CHIPLOGIC

Overview

ChipLogic's I2C IP is a synthesizable IP fully compliant with the I2C bus specification 6.0. It implements APB based host interface. The IP can be configured as Master or Slave. It supports features to integrate into a multi-master multi-slave system. It supports normal/extended addressing. In Master mode, the I2C IP initiates transfer, detects and generates response, implements arbitration, clock synchronization and error handling. In slave mode, it reacts to requests from Master to accept data and generate response, implements error handling.



Block Diagram: I2C Controller

Block Description

- **APB :** The IP uses a APB bus to integrate into a host system. Combined with registers accessed over APB Slave, it allows configuration, control and status exchange between IP and host system.
- **TX/RX FSMs**: For Transmit and Receive /control flow
- **IO Buffer Control**: Generates controls for io-buffers at all supported speeds

Features

- Compliant with I2C specification version 6.0
- Configurable as Master or Slave
- Speeds : Standard, Fast, Fast-Mode Plus, High Speed and Ultra Fast mode
- Addressing : 7-bit and 10 bit modes
- Data arbitration and clock synchronization support
- General call addressing support in slave mode
- Supports all reserved addresses
- Simple register host interface over APB Slave
- Configurable Timing
- Parameters

Language and Methodology

- System Verilog

Deliverables

- Synthesizable, configurable RTL code in Verilog HDL
- User guide
- UVM based testbench to demonstrate functionality of IP
- Synthesis scripts
- Reports – Verification, Coverage, STA

For more information on our Semiconductor IP's reach out to us at:
sales@chiplogictech.com I www.chiplogictech.com