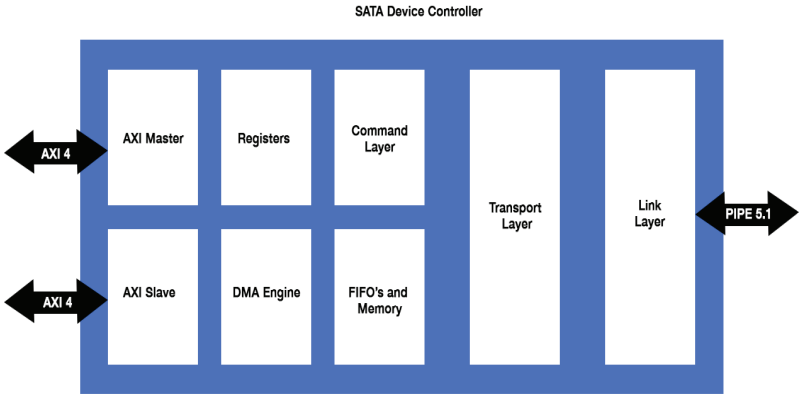
SATA DEVICE CONTROLLER IP

CHIPLOGIC

Overview

ChipLogic's SATA Device Controller IP is compliant with the SATA bus specification 3.4. It implements standard Protocol Layer and Link Layer over Pipe 4.1 Interface. It uses a custom programmable list processor based data interface to implement standard commands with a mechanism to extend support for vendor specific commands. Implements AXI based host interface.



Block Description

- **Command Layer Controller :** Implements custom register interface and data structure to implement sata device commands
- **AXI Master /Slave** : For easy integration with Host Systems
- **Registers and DMA Engine**: For control, data and status exchange. Implements scatter-gather based list processor data transfers. It is configurable for multiple ports and has dedicated DMA as well as register set for each port.
- **Transport and Link Layers:** Supports all standard and configurable features. It connects to an external SATA-PHY over a standard PIPE5.1 interface.

Features

- Compliant with SATA 3.4
- Supports AXI-4 with 32-bit and 64-bit data interface
- PIPE 5.1 interface, 32-bit data bus, backward compatible with earlier versions
- Supports 1.5Gbps, 3.0 Gbps and 6 Gbps
- 32-bit and 64-bit addressing
- Scatter-gather and DMA
- Partial, Slumber and DevSleep modes
- NCQ support
- Configurable Timing
- Interrupts

Language and Methodology

- Verilog

Deliverables

- Synthesizable, configurable RTL code in Verilog HDL
- User guide
- UVM based testbench to demonstrate functionality of IP
- Synthesis scripts
- Reports – Verification, Coverage, STA

For more information on our Semiconductor IP's reach out to us at:
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