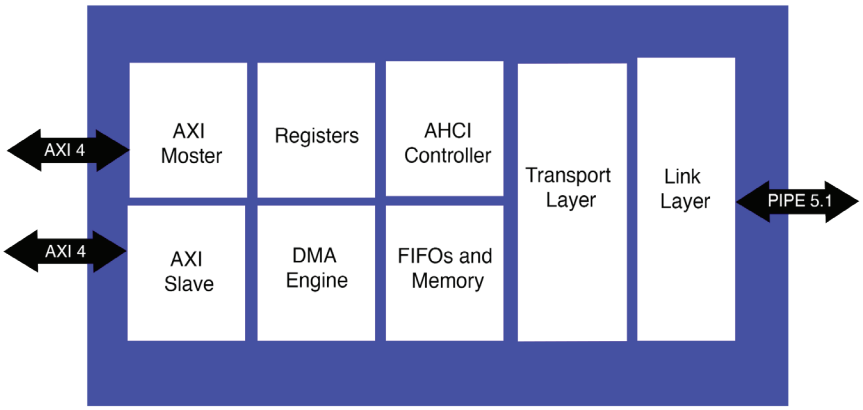
SATA HOST CONTROLLER IP

CHIPLOGIC

Overview

ChipLogic's SATA Host Controller IP is compliant with the SATA busspecification 3.4. It implements Host application layer, transport layer and link layers. It uses AHCI 1.3.1 based software interface



Block Diagram: SATA Host Controller

Block Description

- **AHCI Controller :** Implements standard register interface and data structure to allow use of Host Bus Adapter with standard software drivers provided with Several Operating Systems
- **AXI Master /Slave** : For easy integration with Host Systems
- **Registers and DMA Engine** : For control, data and status exchange.Implements scatter-gather based list processor data transfers. It is configurable for multiple ports and has dedicated DMA as well as register set for each port.
- **Transport and Link Layers** : Supports all standard and configurable features. It connects to an external SATA-PHY over a standard PIPE5.1 interface.

Features

- Compliant with SATA 3.4 and AHCI 1.3.1
- Supports AXI-4 with 32-bit and 64-bit data interface
- PIPE 5.1 interface, 32-bit data bus, backward compatible with earlier versions
- Supports 1.5Gbps, 3.0 Gbps and 6 Gbps
- 32-bit and 64-bit addressing
- Scatter-gather and DMA
- Partial, Slumber and DevSleep modes
- NCQ support
- Interrupts

Language and Methodology

- Verilog

Deliverables

- Synthesizable, configurable RTL code in
- Verilog HDL
- User guide
- UVM based testbench to demonstrate
- functionality of IP
- Synthesis scripts
- Reports – Verification, Coverage, STA

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